Adiabatic Logic Circuits: A Retrospect

Deepti Shinghal
Department of E & C Engg., M.I.T.
Moradabad, UP, INDIA
E-mail: shinghaldeepti0@gmail.com

Amit Saxena
Department of E & C Engg., M.I.T.
Moradabad, UP, INDIA
E-mail: amitssaksena@gmail.com

Arti Noor
Department of M.Tech.
VLSI Design Group, C-DAC, Noida,
UP, INDIA

ABSTRACT

With ever-increasing growth in VLSI technologies the number of gates per chip area is constantly increasing, while the gate switching energy does not decrease at the same rate, so the power dissipation rises and heat removal becomes more difficult and expensive. Then, to limit the power dissipation adiabatic operation promises large reductions of power consumption because it does not dissipate energy. This paper reviews different types of adiabatic logic families. First, adiabatic logic circuits working principle is discussed. Next, adiabatic switching and how it can be used to conserve power is discussed. Also reviewed is an adiabatic logic gate alongwith its circuit. Finally, adiabatic logic family is covered, which can be classified as fully and partially adiabatic alongwith discussion circuit diagram and details of each. This review also covers some important future research directions.

Keywords: Adiabatic circuit, charge recycling, low energy, no dissipation.

I. INTRODUCTION

New generations of processing technology are being developing while present generation of devices are at very safe distance from fundamental physical limits. Need for low power VLSI chips arise from such evolution forces of integrated circuits. The Intel 4004 microprocessor, developed in 1971, had 2300 transistors that dissipated about 1 watt of power and at 1 MHz frequency. After that Pentium comes in 2001, which has 42 million transistors, dissipating 65 watts of power at a frequency of 2.4 GHz. If power density rises in this exponential way increase continuously, a microprocessor designed a few years later, would have the same power as that of the nuclear reactor. Such high power density introduces reliability concerns such as, electro migration, thermal stresses and hot carrier induced device degradation, resulting in the loss of performance. Another factor that fuels the need for low power chips is the increased market demand for portable consumer electronics powered by batteries. The craving for smaller, lighter and more durable electronic products indirectly translates to low power requirements. Battery life is becoming a product differentiator in many portable devices.

Being the heaviest and biggest component in many portable systems, batteries have not experienced the similar rapid density growth compared to the electronic circuits. The main source of power dissipation in these high performance battery-portable digital systems running on batteries such as notebook computers, cellular phones and personal digital assistants are gaining prominence. For these systems, low power consumption is a prime concern, because it directly affects the performance by having effects on battery longevity.

In this situation, low power VLSI design has assumed great importance as an active and rapidly developing field.

Power consumption is one of the basic parameters of any kind of integrated circuit (IC). Power and performance are always traded off to meet the system requirements. Power has a direct impact on the system cost.

The rest of the paper is organized as follows. Section 2 discusses about adiabatic logic circuits and Section 3 describes various adiabatic logic families. In Section 4 we explores fully adiabatic logic and finally Sections 5 and 6 provides conclusion and future work respectively.

II. ADIABATIC LOGIC CIRCUITS

2.1. CMOS Logic Circuits Principal

Power dissipation in conventional CMOS circuits primarily occurs during device switching. As shown in Fig. 1, both PMOS and NMOS transistors can be modelled by including an ideal switch in series with a resistor in order to represent the effective channel resistance of the switch and the interconnect resistance.

The pull-up and pull-down networks are connected to the node capacitance $C_L$, which is referred to as the load capacitance in this paper.

When the logic level in the system is “1” there is a sudden flow of current through $Q = C_L V_{dd}$ is the charge supplied by the positive power supply rail for charging $C_L$ to $V_{dd}$. Hence, the energy drawn from the power supply is $Q V_{dd} = C_L V_{dd}^2$. If it is assumed that the energy drawn from the power supply is
equal to that supplied to $C_L$, the energy stored in $C_L$ becomes one-half the supplied energy, i.e.

$$E_{\text{stored}} = 0.5 \ C_L \ V_{dd}^2 \quad (1)$$

The remaining energy is dissipated in $R$. The same amount of energy is dissipated during discharging in the NMOS pull-down network when the logic level in the system is “0.” Therefore, the total amount of energy dissipated as heat during charging and discharging is

$$E_{\text{total}} = E_{\text{charge}} + E_{\text{discharge}} \quad (2)$$

$$= 0.5 C_L \ V_{dd}^2 + 0.5 C_L \ V_{dd}^2$$

$$= C_L \ V_{dd}^2$$

**Figure 1:** A Conventional CMOS model along with charging and discharging

From the above equation, it is apparent that the energy consumption in a conventional CMOS circuit can be reduced by reducing $V_{dd}$. By decreasing the switching activity in the circuit, the power consumption ($P = \text{d}E/\text{d}t$) can also be proportionally suppressed.

### 2.2. Adiabatic Logic Circuits Principal

Adiabatic switching is commonly used to minimize energy loss during charging/discharging. The word “adiabatic” (Greek adiabatos, which means impassable) indicates a state change that occurs without heat loss or gain. During adiabatic switching, all the nodes are charged or discharged at a constant current in order to minimize power dissipation. This is accomplished by using AC power supplies to initially charge the circuit during specific adiabatic phases and then discharge the circuit to recover the supplied charge. The principle of adiabatic switching can be best explained by contrasting it with the conventional dissipative switching technique. Figure 2 shows the manner in which energy is dissipated during a switching transition in adiabatic logic circuits.

**Figure 2:** An Adiabatic logic model along with charging and discharging

In contrast to conventional charging, the rate of switching transition in adiabatic circuits is decreased because of the use of a time-varying voltage source instead of a fixed voltage supply. Each voltage changes with time, as demonstrated in Fig. 3. The peak current in adiabatic circuits can be significantly reduced by ensuring uniform charge transfers over the entire available time. Hence, if $I'$ is considered as the average of the current flowing to $C_L$, the overall energy dissipation during the transition phase can be reduced in proportion as follows [2]:

Theoretically, during adiabatic charging, when the time for the driving voltage $\phi$ to change from 0 V to $V_{dd}$, $T_p$ is long, power dissipation is nearly zero. When $\phi$ changes from HIGH to LOW in the pulldown network, discharging via the nMOS transistor occurs. From Eq. (2), it is apparent that when power dissipation is minimized by decreasing the rate of switching transition, the system draws some of the energy that is stored in the capacitors during a given computation step and uses it in subsequent computations. The signal energy may be recycled instead of dissipated as heat [2]. It must be noted that systems based on the above mentioned theory of charge recovery are not necessarily reversible.

### 2.3 A Simple Adiabatic Logic Gate

In this we will examine simple circuit configurations which can be used for adiabatic switching. A general circuit topology for the conventional CMOS gates and adiabatic counterparts is shown in Figure 3. To convert a conventional CMOS logic gate into an adiabatic gate, the pull-up transistor and the pull-down transistor networks must be replaced with complementary transmission-gate (T-gate). The T-gate network implementing the pull-up function is used to drive the true output of the adiabatic gate, while the T-gate network implementing the pulldown function drives the complementary output node.

**Figure 3:** A Simple Adiabatic Logic Gate

Note that all the inputs should also be available in complementary form.

Both the pull-up and pull-down networks in the adiabatic logic circuit are used for charging as well as discharging the output node capacitance, which ensures that the energy stored at the output node can be retrieved by the power supply, at the end of each cycle shown in Figure 4. To allow adiabatic operation, the DC voltage source of the original circuit must be replaced by a varying power supply with the ramped voltage output.
The necessary circuit modifications which are used to convert a conventional CMOS logic circuit into an adiabatic logic circuit increase the device count by a factor of two or even more.

III. ADIABATIC LOGIC FAMILIES

Adiabatic logic circuits classified into two types: (a) Quasi/Partial Adiabatic Logic Circuits (b) Full Adiabatic Logic Circuits

(a) Quasi/Partial Adiabatic Logic Circuits: Quasi-adiabatic circuits have simple architecture and power clock system. The adiabatic loss occurs when current flows through non-ideal switch, which is proportional to the frequency of the power-clock.

Popular Partially Adiabatic families include the following:
(i) Efficient Charge Recovery Logic (ECRL).
(ii) 2N-2N2P Adiabatic Logic.
(iii) Positive Feedback Adiabatic Logic (PFAL).
(iv) NMOS Energy Recovery Logic (NERL).
(v) Clocked Adiabatic Logic (CAL).
(vi) True Single-Phase Adiabatic Logic (TSEL).
(vii) Source-coupled Adiabatic Logic (SCAL).

(b) Full Adiabatic Logic Circuits: Full-adiabatic circuits have no non-adiabatic loss, but they are much more complex than quasi-adiabatic circuits. All the charge on the load capacitance is recovered by the power supply. Fully adiabatic circuits face a lot of problems with respect to the operating speed and the inputs power clock synchronization.

Some Fully adiabatic logic families include:
(i) Pass Transistor Adiabatic Logic (PAL).
(ii) Split- Rail Charge Recovery Logic (SCRL).

3.1 Efficient Charge – Recovery Logic (ECRL)

Efficient Charge – Recovery Logic (ECRL) proposed by Moon and Jeong [13], shown in Figure 5, uses cross-coupled PMOS transistors. It has the structure similar to Cascode Voltage Switch Logic (CVSL) with differential signalling.

It consists of two cross-coupled transistors M1 and M2 and two NMOS transistors in the N-functional blocks for the ECRL adiabatic logic block [13].

An AC power supply $pwr$ is used for ECRL gates, so as to recover and reuse the supplied energy. Both out and /out are generated so that the power clock generator can always drive a constant load capacitance independent of the input signal. A more detailed description of ECRL can be found in [13]. Full output swing is obtained because of the cross-coupled PMOS transistors in both precharge and recover phases. But due to the threshold voltage of the PMOS transistors, the circuits suffer from the non-adiabatic loss both in the precharge and recover phases. That is, to say, ECRL always pumps charge on the output with a full swing. However, as the voltage on the supply clock approaches to $|V_{tp}|$, the PMOS transistor gets turned off.

So the recovery path to the supply clock to the supply clock is disconnected, thus, resulting in incomplete recovery. $V_{tp}$ is the threshold voltage of PMOS transistor. The amount of loss is given as

$$E_{ECRL} = C|V_{tp}|^2/2$$

(3)

Thus, from Equation (3), it can be inferred that the non-adiabatic energy loss is dependent on the load capacitance and independent of the frequency of operation.

The ECRL circuits are operated in a pipelining style with the four-phase supply clocks. When the output is directly connected to the input of the next stage (which is a combinational logic), only one phase is enough for a logic value to propagate. However, when the output of a gate is fed back to the input, the supply clocks should be in phase. A latch is one of the simplest cases which have a feedback path. The input signals propagate to the next stage in a single phase, and the input values are stored in four phases (1-clock) safely.

Let us assume in is at high and inb is at low. At the beginning of a cycle, when the supply clock ‘pwr’ rises from zero to VDD, out remains at a ground level, because in turns on F-tree (NMOS logic tree). /out follows pwr through M1. When pwr reaches VDD, the outputs hold valid logic levels. These
values are maintained during the hold phase and used as inputs for the evaluation of the next stage. After the hold phase, pwr falls down to a ground level, out node returns its energy to pwr so that the delivered charge is recovered. Thus, the clock pwr acts as both a clock and power supply.

A major disadvantage of this circuit is the existence of the coupling effects, because the two outputs are connected by the PMOS latch and the two complementary outputs can interfere each other.

### 3.2 Positive Feedback Adiabatic Logic (PFAL)

The partial energy recovery circuit structure named Positive Feedback Adiabatic Logic (PFAL) [15] has been used, since it shows the lowest energy consumption if compared to other similar families, and a good robustness against technological parameter variations. It is a dual-rail circuit with partial energy recovery. The general schematic of the PFAL gate is shown in Figure 6. The core of all the PFAL gates is an adiabatic amplifier, a latch made by the two PMOS M1-M2 and two NMOS M3-M4, that avoids a logic level degradation on the output nodes out and out. The two n-trees realize the logic functions. This logic family also generates both positive and negative outputs. The functional blocks are in parallel with the PMOSFETs of the adiabatic amplifier and form a transmission gate. The two n-trees realize the logic functions. This logic family also generates both positive and negative outputs.

The two major differences with respect to ECRL are that the latch is made by two PMOSFETs and two NMOSFETs, rather than by only two PMOSFETs as in ECRL logic, and that the functional blocks are in parallel with the transmission PMOSFETs. Thus the equivalent resistance is smaller when the capacitance needs to be charged.

### 3.3 Clocked Adiabatic Logic (CAL)

CAL is a dual-rail logic that operates from a single-phase AC power-clock supply [17]. In the adiabatic mode, the power-clock supply waveform is generated using an on-chip switching transistor and a small external inductor between the chip and a low-voltage dc supply.

The basic CAL gate, the inverter, is shown in Figure 7. Cross-coupled CMOS inverters, transistors M1 – M4, provide memory function. In order to realize an adiabatic inverter and other logic functions with a single power clock, an auxiliary timing control clock signal CX has been introduced, as shown in above Figure 7. This signal controls the transistors that are in series with the logic trees represented by the functional blocks F and /F. The CX-enabled devices allow operation with a single power clock pwr.

### 3.4 NMOS Energy Recovery Logic (NERL)

NMOS energy recovery logic (NERL), which uses NMOS transistors only and a simpler 6-phase clocked power. Its area overhead and energy consumption are smaller, compared with the other fully adiabatic logics. We employed bootstrapped NMOS switches to simplify the NERL circuits. With the simulation results for a full adder, we confirmed that the NERL circuit consumed substantially less energy than the other adiabatic logic circuits at low-speed operation. NERL is more suitable than the other adiabatic logic circuits for the applications that do not require high performance but low energy consumption.

### 3.5 True Single-Phase Adiabatic Logic (TSEL)

TSEL is a partially adiabatic circuit family related to 2N2P, 2N-2N2P, and CAL. Power is supplied to TSEL gates by a single phase sinusoidal power-clock. Cascades are composed
of alternating PMOS and NMOS gates. Two DC reference voltages ensure high-speed and high-efficiency operation. They also enable the cascading of TSEL gates in an NP-domino style. In comparison with corresponding adders in Alternative logic styles and minimum possible supply voltages, TSEL is more energy efficient across a broad range of operating frequencies. Specifically for clock frequencies ranging from 10MHz to 200MHz. TSEL is the first energy-recovering logic family that operates with a single-phase sinusoidal clocking scheme. Both TSEL and SCAL gates are dual-rail and always present a balanced load to the clock generator, regardless of the particular data computed. Moreover, they are both functionally complete.

3.6 Source-Coupled Adiabatic Logic (SCAL)
SCAL is a partially adiabatic, dynamic logic family. SCAL retains all of TSEL’s positive features, including single-phase power-clock operation. Moreover, it achieves energy efficient operation across a broad range of operating frequencies by using an individually tunable current source at each gate. SCAL achieves increased energy efficiency by using a tunable current source to control the rate of charge flow into or out of each gate. Our adiabatic circuitry avoids a number of problems associated with multiple power-clock schemes, including increased energy dissipation, layout complexity in clock distribution, clock skew, and multiple power-clock generators.

3.7 2N-2P Adiabatic Logic Family
The schematic of the 2N-2P inverter gate is shown in Figure 11. Initially, input ‘in’ is high and input ‘/in’ is low. When power clock (pclk) rises from zero to V_{DD}, since F is on so output ‘/out’ remains ground level. Output ‘/out’ follows the pclk. When pclk reaches at V_{DD}, outputs ‘out’ and ‘/out’ hold logic value zero and V_{DD} respectively. This output values can be used for the next stage as an inputs. Now pclk falls from V_{DD} to zero, ‘/out’ returns its energy to pclk hence delivered charge is recovered. ECRL uses four phase clocking rule to efficiently recover the charge delivered by pclk. For detailed study follow the reference [4].

3.8 2N-2N2P Adiabatic Logic
The 2N-2N2P logic family was derived from 2N-2P in order to reduce the coupling effect. The major difference with respect to 2N-2P is that the latch is made by two pMOSFETs and two nMOSFETs, rather than by only two pMOSFETs as in 2N-2P. The additional cross-coupled nMOSFET switches lead to non-floating outputs for a large part of the recovery phase.

IV. FULLY ADIABATIC LOGIC

4.1 Pass Transistor Adiabatic Logic (PAL)
PAL is a dual-rail adiabatic logic with a relatively low gate complexity that operates with a two-phase power clock. A PAL gate consists of true and complementary pass transistor NMOS functional blocks (f, /f), and a cross coupled PMOS latch (Mp1, Mp2), as illustrated by the example of Figure 12, which shows the implementation of an AND-OR gate: Q = A.B + C. The power is supplied through a sinusoidal power-clock (PC). When PC starts rising from low, input states make a conduction path from the power clock (PC) through one of the functional blocks to the corresponding output node and allow it to follow the power clock. The other node will be tri-state and kept close to OV by its load capacitance. This in turn causes one of the PMOS transistors to conduct and charge the node that should go to one state, up to the peak of PC. The output state is valid at around the top of the power clock.
The power clock will then ramp down toward zero, recovering the energy stored on the output node capacitance.

Pass Transistor adiabatic logic (PAL) family exhibits considerable improvements in terms of energy savings and switching noise characteristics, it has the disadvantages of higher supply voltage and lower speed of operation.

4.2 Split Charge Recovery Logic (SCRL)
Split-Level Charge Recovery Logic (SCRL), within which the transfer of charge between the nodes occurs quasi-statically. Operating quasi-statically, these logic families have an energy dissipation that drops linearly with operating frequency, i.e., their power consumption drops quadratically with operating frequency as opposed to the linear drop of conventional CMOS. The circuit techniques in these new families rely on constructing an explicitly reversible pipelined logic gate, where the information necessary to recover the energy used to compute a value is provided by computing its logical inverse. Information necessary to uncompute the inverse is available from the subsequent inverse logic stage. We demonstrate the low energy operation of SCRL by presenting the results from the testing of the first fully quasi static 8 × 8 multiplier chip (SCRL-1) employing SCRL circuit techniques.

V. CONCLUSION
Our study showed that adiabatic logic circuits provide a method of decreasing the energy dissipation when compared with conventional logic switching under certain circumstances. With adiabatic circuits all input signals must undergo a controlled transition in the form of a ramp, unlike the conventional logic switching where only the input signals which have different final logic state change. To reduce energy dissipation, logic switching cannot be instantaneous but must be gradual instead. With the circuits examined in this paper, there is a lower limit to the energy dissipation beyond which no significant improvements can be achieved for increasing rise/fall times. This limitation is mainly due to the finite threshold voltage of the MOS transistors and possibly to a lesser extent, the non-linear characteristics of the MOS channel resistance.

It was also observed that the fully adiabatic circuits reduce the power consumption significantly but they are very complex to design and although the partially adiabatic circuits are not as efficient as fully adiabatic circuits in terms of power consumption but they reduce the circuit complexity and conserve the power. So we can say that partially adiabatic circuits are fair compromise between the power consumption and complexity trade off.

VI. FUTURE WORK
From the study it was found that the adiabatic logic circuits can play a significant role in designing applications where power conservation is of prime importance such as in high performance, hand held and portable digital systems running on batteries such as notebook computers, cellular phones and personal digital assistants. With the adiabatic switching approach, the circuit energies are conserved rather than dissipated as heat. In future research depending on the application and the system requirements, a suitable adiabatic circuit design approach can be selected and analyzed to reduce the power dissipation of such systems.

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